

WHAT IS CLAIMED IS:

1 1. A method of verifying correct operation of a forward error correction
2 decoder, comprising the steps of:
3 programmably selecting a desired number of errors for insertion into a
4 plurality of data signals;
5 defining a plurality of code words of the data signals;
6 inserting into one of the data signals the desired number of errors using an
7 error insertion circuit;
8 repeating said inserting step in an iterative fashion to insert into different data
9 signals the desired number of errors wherein the errors are placed
10 within the code words of the data signals at different location
11 permutations for each data signal;
12 transmitting the data signals with the inserted errors to a receiver; and
13 determining that the data signals received at the receiver contain the inserted
14 errors.

1 2. The method of Claim 1 wherein said repeating step cycles through all
2 possible permutations of all the code word locations.

1 3. The method of Claim 1 wherein the error insertion circuit operates in one of
2 a plurality of modes, including a short frame mode for shorter permutation cycles, and
3 further comprising the steps of:
4 selecting the short frame mode for operation; and
5 in response to said selecting step, limiting said repeating step to cycle through
6 less than all possible permutations of all the code word locations.

1 4. The method of Claim 1 wherein:
2 the data signal is a SONET data signal having nine rows; and
3 said repeating step results in the insertion of errors in 32 code words defined
4 within each of the nine SONET rows.

1 5. The method of Claim 1 wherein said repeating step stops after one
2 permutation cycle in response to the further step of programming the error insertion
3 circuit for single cycle operation.

1 6. The method of Claim 1 wherein said determining step includes the step of
2 examining an error accumulator count in the receiver to match a number of
3 accumulated errors with the number of inserted errors.

1 7. The method of Claim 6 wherein said examining step matches the number
2 of accumulated errors with the number of inserted errors using a modulo function.

1 8. The method of Claim 1 wherein:
2 the error insertion circuit includes an error mask for selectively preventing
3 insertion of one or more of the errors; and
4 said repeating step is limited to inserting errors in selected code words based
5 on the error mask.

1 9. The method of Claim 1 wherein said repeating step includes the step of
2 tracking the location of a current code word in which an error is being inserted.

1 10. The method of Claim 9 wherein said tracking step includes the step of
2 incrementing one or more registers in a location counter having at least first, second,
3 and third registers, the first register corresponding to a column location, the second
4 register corresponding to an index location, and the third register corresponding to a
5 byte location.

6 11. A method of injecting a plurality of errors into a SONET data stream,
7 comprising the steps of:
8 programming an error insertion circuit to select a desired number of errors for
9 insertion into a plurality of successive SONET data signals each
10 having a plurality of rows;
11 defining a plurality of forward error correction (FEC) code words within each
12 of the rows of the SONET data signals;

13 inserting the desired number of errors into a first one of the SONET data
14 signals at a first code word permutation location, using the error
15 insertion circuit;
16 tracking the first code word permutation location in response to said step of
17 inserting the desired number of errors into the first SONET data signal;
18 and
19 inserting the desired number of errors into a second one of the SONET data
20 signals at a second code word permutation location, using the error
21 insertion circuit, and in response to said tracking step.

1 12. The method of Claim 11 further comprising the step of programming the
2 error insertion circuit for single cycle operation.

1 13. The method of Claim 11 further comprising the step of programming the
2 error insertion circuit for short frame mode operation.

1 14. The method of Claim 11 wherein said tracking step includes the step of
2 incrementing one or more registers in a location counter having at least first, second,
3 and third registers, the first register corresponding to a SONET column location, the
4 second register corresponding to an index location, and the third register
5 corresponding to a byte location, the index and byte locations together representing a
6 SONET byte location.

1 15. The method of Claim 11 wherein said inserting steps occur after the
2 further step of scrambling the SONET data signals.

1 16. An error injection circuit comprising:
2 means for selectively programming a desired number of errors for insertion
3 into a plurality of data signals;
4 means for defining a plurality of code words of the data signals; and
5 means for repeatedly inserting the desired number of errors into different ones
6 of the data signals at different code word permutation locations.

1 17. The error injection circuit of Claim 16 wherein said inserting means cycles
2 through all possible permutations of all the code word locations.

1 18. The error injection circuit of Claim 16 further comprising means for
2 selecting a short frame mode of operation, wherein said inserting means limits
3 insertion of the errors to cycle through less than all possible permutations of all the
4 code word locations when the short frame mode of operation is selected.

1 19. The error injection circuit of Claim 16 wherein:
2 the data signal is a SONET data signal having nine rows; and
3 said inserting means inserts errors in 32 code words defined within each of the
4 nine SONET rows.

1 20. The error injection circuit of Claim 16 further comprising means for
2 selecting single cycle operation, wherein said inserting means stops inserting errors
3 after one permutation cycle when the single cycle operation is selected.

1 21. The error injection circuit of Claim 16 further comprising error mask
2 means for selectively preventing insertion of one or more of the errors, wherein said
3 inserting means inserts errors in selected code words based on said error mask means.

1 22. The error injection circuit of Claim 16 wherein said insertion means
2 includes means for tracking the location of a current code word in which an error is
3 being inserted.

1 23. The error injection circuit of Claim 16 wherein said tracking means
2 increments one or more registers in a location counter having at least first, second,
3 and third registers, the first register corresponding to a column location, the second
4 register corresponding to an index location, and the third register corresponding to a
5 byte location.

1 24. An OC-192 input/output card comprising:
2 four OC-48 processors; and

3 an OC-192 front-end application-specific integrated circuit (ASIC) connected
 4 to said four OC-48 processors, said OC-192 front-end ASIC including
 5 a transmitter having means for interleaving four OC-48 signals to
 6 create an OC-192 signal, and means for encoding forward error
 7 correction (FEC) codes in each of the four OC-48 signals,
 8 a receiver having means for de-interleaving an OC-192 signal to create
 9 four OC-48 signals, and means for decoding FEC codes in the
 10 OC-192 signal, and
 11 means for verifying correct operation of said encoding means and said
 12 decoding means.

1 25. The OC-192 input/output card of Claim 24 wherein said verifying means
 2 includes:

3 means for selectively programming a desired number of errors for insertion
 4 into a plurality of successive SONET data signals;
 5 means for defining a plurality of FEC code words of the SONET data signals;
 6 means for repeatedly inserting the desired number of errors into different ones
 7 of the SONET data signals at different code word permutation
 8 locations;
 9 means for routing the SONET data signals with the inserted errors from said
 10 transmitter to said receiver; and
 11 means for determining that the SONET data signals received at said receiver
 12 contain the inserted errors.

1 26. The OC-192 input/output card of Claim 25 wherein said inserting means
 2 cycles through all possible permutations of all the FEC code word locations.

1 27. The OC-192 input/output card of Claim 25 further comprising means for
 2 selecting a short frame mode of operation, wherein said inserting means limits
 3 insertion of the errors to cycle through less than all possible permutations of all the
 4 code word locations when the short frame mode of operation is selected.

1 28. The OC-192 input/output card of Claim 25 further comprising means for
2 selecting single cycle operation, wherein said inserting means stops inserting errors
3 after one permutation cycle when the single cycle operation is selected.

1 29. The OC-192 input/output card of Claim 25 further comprising error mask
2 means for selectively preventing insertion of one or more of the errors, wherein said
3 inserting means inserts errors in selected code words based on said error mask means.

1 30. The OC-192 input/output card of Claim 25 wherein said insertion means
2 includes means for tracking the location of a current code word in which an error is
3 being inserted.

1 31. The OC-192 input/output card of Claim 24 wherein said programming
2 means allows from one to four errors to be inserted in a given SONET data signal.

1 32. The OC-192 input/output card of Claim 24 wherein said encoding means
2 and said decoding means use a triple-error correcting Bose-Chaudhuri-Hocquenghem
3 (BCH) code.

1 33. The OC-192 input/output card of Claim 25 wherein said determining
2 means includes an error accumulator located in said receiver, and means for
3 examining an error accumulator count of the error accumulator to match a number of
4 accumulated errors with the number of inserted errors.

1 34. The OC-192 input/output card of Claim 30 wherein said tracking means
2 increments one or more registers in a location counter having at least first, second,
3 and third registers, the first register corresponding to a SONET column location, the
4 second register corresponding to an index location, and the third register
5 corresponding to a byte location, the index and byte locations together representing a
6 SONET byte location.

1 35. The OC-192 input/output card of Claim 34 wherein said tracking means
2 contains 10 location counters, including:
3 a first location counter for tracking a location of a first error bit;
4 second and third location counters nested together for tracking a location of a
5 second error bit;
6 fourth, fifth and sixth location counters nested together for tracking a location
7 of a third error bit; and
8 seventh, eighth and ninth location counters nested together for tracking a
9 location of a fourth error bit.

1 36. The OC-192 input/output card of Claim 33 wherein said error accumulator
2 accumulates both corrected errors and uncorrectable errors.

1 37. An error injection circuit comprising:
2 an error selection interface which programs a desired number of errors for
3 insertion into a plurality of data signals;
4 an encoding circuit which defines a plurality of code words of the data signals;
5 and
6 a location counter which increments through a plurality of locations in each of
7 the code words and inserts the desired number of errors into different
8 ones of the data signals at different code word permutation locations.

1 38. The error injection circuit of Claim 37 wherein said location counter
2 means cycles through all possible permutations of all the code word locations.

1 39. The error injection circuit of Claim 37 wherein:
2 the data signal is a SONET data signal having nine rows; and
3 said inserting means inserts errors in 32 code words defined within each of the
4 nine SONET rows.

1 40. The error injection circuit of Claim 37 further comprising an error mask
2 which selectively prevents insertion of one or more of the errors in selected code
3 words